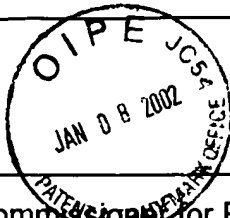


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**U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE**

Commissioner for Patents  
Washington, DC 20231

Attorney Docket No.

2207/11239

Application Number  
09/895,526

Filing Date  
June 29, 2001

Examiner  
Unknown

Group Art Unit  
2121

Application Title  
**A FAST SINGLE PRECISION FLOATING POINT  
ACCUMULATOR USING BASE 32 SYSTEM**

Inventor(s)  
Yatin HOSKOTE, et al.

Technology Center 2000  
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Renee Brogdon

**INFORMATION DISCLOSURE STATEMENT  
WITHIN THREE MONTHS OF FILING OR BEFORE  
MAILING OF FIRST OFFICE ACTION (37 CFR 1.97(b))**

In accordance with the duty of disclosure under 37 CFR §1.56 and in conformance with the procedures of 37 CFR §1.97 and 1.98 and MPEP §609, Applicant hereby brings the attached references to the attention of the Examiner. These references are listed on the attached PTO Form 1449. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

A copy of each reference listed on the PTO Form 1449 is attached.

The Commissioner is authorized to charge any fees required or credit any overpayment in connection with this correspondence to Deposit Account **11-0600**.

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Date: November 12, 2001

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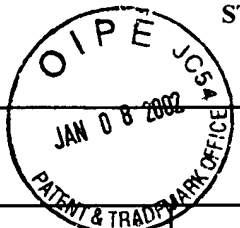
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Form PTO-1449 (modified)  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT(S)' INFORMATION DISCLOSURE STATEMENT</b>			Attorney Docket No. 2207/11239		Serial No. 09/895,526	
			Applicant Yatin HOSKOTE, et al.			
			Filing Date June 29, 2001		Group Art Unit 2121	
COPY OF PAPERS ORIGINALLY FILED			U. S. PATENT DOCUMENTS			
EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE

- If pertinent

EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	A. Beaumont-Smith, et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures" IEEE, 1999
	Erdem Hokenek, et al., "Second-Generation RISC Floating Point with Multiply-Add Fused", IEEE Journal of Solid-State Circuits, Vol. 25, No. 5, October 1990, pp 1207-1213
	Fayez Elguibaly, "A Fast Parallel Multiplier-Accumulator Using the Modified Booth Algorithm", IEEE Transactions on Circuits and Systems -- II: Analog and Digital Signal Processing, Vol. 47, No. 9, September 2000, pp 902-908.
	G. Panneerselvam and B. Nowrouzian, "Multiply-Add Fused RISC Architectures for DSP Applications", IEEE Pac Rim '93, pp 108-111
	Zhen Luo and Margaret Martonosi, "Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware with Delayed Addition Techniques" IEEE Transactions on Computers, Vol. 49, No. 3, March 2000, pp 208-218